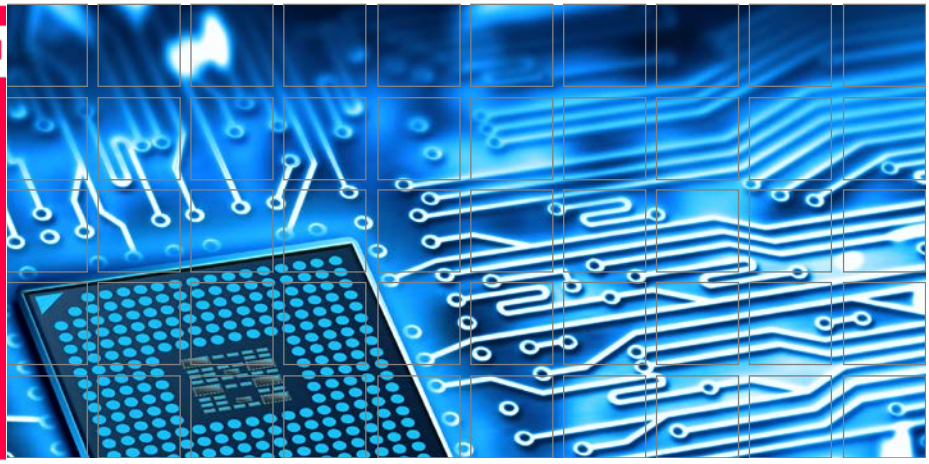
Institute of Electronics





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# Selected Topics of Advanced Analog Chip Design

Winter semester 2015/2016

The lectures will be given by internationally recognized experts and cover selected topics in the field of analog chip design.

Subjects that will be covered:
EMC, ESD, radiation hardness, component mismatch, energy harvesting, robust automotive IC design, device mismatch characterization, advanced CMOS output drivers, …

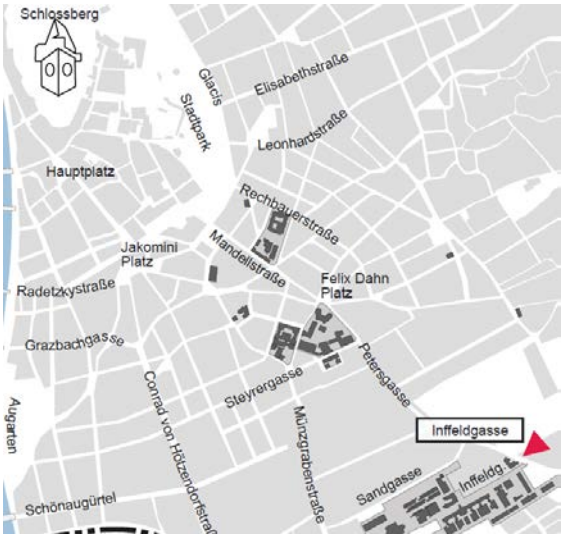
date: December 2015 and January 2016
place: TU Graz, Inffeldgasse

# Course dates

| Date | From | To | Place | Lecturer | Topic |
|---|---|---|---|---|---|
| 03.12.2015 | 11:15 | 12:00 | HS i6 | Christoph Steffan | Energy Harvesting - Feasibility of Chip Integration |
| 03.12.2015 | 13:15 | 14:00 | HS i5 | Harald Dillersberger | Efficiently Harvesting Energy from Temperature Differences in order to power Wireless Systems |
| 03.12.2015 | 14:00 | 14:45 | HS i5 | Robert Kappel | Thermoelectric Energy Harvesting and the Challenge of Operating CMOS Logic Gates in Deep Sub-threshold Region |
| 07.12.2015 | 14:00 | 15:30 | HS i6 | Dr. Bernd Deutschmann | Advanced CMOS Output Drivers to Reduce the Electromagnetic Emission |
| 14.12.2015 | 15:00 | 16:30 | HS i5 | Dr. Timm Ostermann | Special Design Issues in RTC and POR Design |
| 17.12.2015 | 08:15 | 09:45 | HS i5 | Dr. Michalowska-Forsyth<br>Varvara Bezhenova | Ionizing Radiation and Radiation Hardness in Analog Integrated Circuits |
| 07.01.2016 | 08:30 | 16:00 | HS FSI1 | Dr. Marcel Pelgrom | A Designer's View on Component Mismatch |
| 11.01.2016 | 13:00 | 16:00 | HS i5 | Anton Klotz<br>Ioannis Syranidis | Analog Modeling with Verilog-A – Part 1 |
| 12.01.2016 | 10:30 | 12:45 | HS i5 | Anton Klotz<br>Ioannis Syranidis | Analog Modeling with Verilog-A – Part 2 |
| 14.01.2016 | 08:30 | 11:30 | HS i15 | Dr. Joost Willemen<br>Filippo Magrini | Introduction to System and Component Level ESD Protection |
| 21.01.2016 | 08:30 | 10:00 | HS i5 | Werner Posch | Device Mismatch Characterization:<br>Basics, Test structures, Measurements, Modeling |
| 27.01.2016 | 14:00 | 18:30 | HS i5 | Paolo del Croce<br>Luca Petruzzi | Robust Design of Smart Power ICs for Automotive Applications |

**HS FSI1** → TU Graz, Inffeldgasse 11/EG **HSi5, HSi6** → TU Graz, Inffeldgasse 25D/1. OG

**HS i15** → TU Graz, Inffeldgasse 18/1. KG




# Lectures in December 2015

### Energy Harvesting - Feasibility of Chip Integration

**Christoph Steffan** TU Graz; Infineon Technologies AG, Graz

Energy Harvesting technologies are fundamental in enabling the realization of self-sustainable and therefore autonomous working devices. In this presentation a short overview about capable energy sources, transducers and converters will be given. The feasibility of chip integration as well as working principles of the transducers and converters will be discussed.

### Efficiently Harvesting Energy from Temperature Differences in order to power Wireless Systems

**Harald Dillersberger** private work together with **Prof. Marcel Meli** (not present) ZHAW, Winterthur

Devices that generate electrical energy from a temperature difference are often used to provide energy autonomy. Since they normally deliver small voltages, the use of a step-up converter is required to get to the needed voltage for the electronics. Several such boosters exist on the market. In the practice, it is often difficult to provide enough energy when the temperature differences are small. It is well known that the impedance of the harvester can strongly influence the performance of the booster and therefore have an impact on the cost of the harvester. In this work, we present a booster architecture that allows a good impedance matching for existing TEG harvesters. The amount of energy harvested for a small temperature difference is high enough to allow the efficient use of small commercial TEGs. We show how this power management system can be combined with very low power electronics to power sensors and communicate using BLE or other wireless systems.

### Thermoelectric Energy Harvesting and the Challenge of Operating CMOS Logic Gates in Deep Sub-threshold Region

**Robert Kappel** ams AG

This lecture gives an overview on thermoelectric energy harvesting in environments of low temperature gradients (e.g. on-body applications) by discussing the thermal and the electrical characteristics of a thermoelectric generator. Operation in such an application scenario requires integrated circuits, which are functional under deep sub-threshold conditions. A simple method to reduce the minimum supply voltage of CMOS logic gates to 90mV at room temperature without the need of special process options or low-VTH devices is therefore introduced in the second part of the talk. Finally, the functionality of this technique is proven by measurement results of basic digital logic cells.

### Advanced CMOS Output Drivers to Reduce the Electromagnetic Emission

**Dr. Bernd Deutschmann** TU Graz

Conventional CMOS output drivers often generate high electromagnetic emission when the output signal is changing its state from high to low and vice versa. In this talk basic concepts of designing advanced output driver topologies in order to significantly reduce the electromagnetic emission of ICs are shown. Based on the design of

conventional output drivers it will be demonstrated how ground bouncing, as one of the major sources of common mode emission, is created, how its amplitude can be calculated and how it can be reduced.
Controlling the slew rate of the output signal is one appropriate measure to reduce ground bouncing as well as the electromagnetic emission. A slew rate controlled output driver that is based on the distributed and weighted technique is used to demonstrate how the emission of an IC can effectively be reduced.

### On-Chip Calibration of Temperature Stable Voltage References

**Dr. Timm Ostermann** Johannes-Kepler-Universität Linz

Within this lecture first the design of a low-power real time clock (RTC) in a standard CMOS process will be discussed.
Different design issues regarding the robustness of the low power RTC will be considered.
The second part of the lecture deals with the design of accurate power on reset circuits (POR).

### Ionizing Radiation and Radiation Hardness in Analog Integrated Circuits

**Dr. Alicja Michalowska** TU Graz

**Varvara Bezhenova** TU Graz

Ionizing radiation can cause various issues in the integrated circuits: from soft errors to permanent performance degradation or even damage. These can become a concern, whether the IC is dedicated to work in harsh environments with high radiation levels, like industrial or space applications, or it is targeted for consumer electronics, exposed only to the background radiation. In the modern highly integrated IC technologies certain effects are more pronounced, because of lower node capacitances, while some others are partially supressed, by the charge carrier tunnelling phenomenon in the nanometer-thick gate oxide. In this lecture main sources of the ionizing radiation will be briefly discussed. Then phenomena occurring in the semiconductor devices in the presence of X-rays or other high energy radiation will be explained. Finally some techniques applicable at the layout and the circuit topology level will be presented to improve the IC robustness.

# Lectures in January 2016

## A Designer's View on Component Mismatch

**Dr. Marcel Pelgrom** Pelgrom Consult

Circuit design greatly depends on the ability to control and reproduce transistor and process parameters. Variation in processing was in the past countered by defining process corners. With the improved control over processing, this batch-to-batch variation is largely under control. Statistical variations between otherwise identical components are generally described by "mis-match" parameters. Analog ICs with differential operation were already heavily affected by mismatch. In today's advanced technologies every circuit from SRAM cell to an I-Q mixer must deal with statistical variations. Understanding and mitigating these effects requires more and more statistical means.

This class will review some of the statistical effects and discuss fundamentals, measurements, technology trends and elaborate on the way analog designers can deal with these issues.

With some exercises the consequences in opamps, bandgap circuits etc will be shown. Lessons from the analog domain provide a starting point for the application in the digital domain, and are also helpful in defining targets for process development and test methodology.

## Analog Modeling with Verilog-A

**Anton Klotz** Cadence Academic Network

**Ioannis Syranidis** Cadence Academic Network

In this course, you use the Virtuoso® Analog Design Environment and Virtuoso Spectre® Circuit Simulator to simulate analog circuits with Verilog-A models. Verilog-A is a high-level language that uses modules to describe the structure and behavior of analog systems and their components. You use the Verilog-A syntax, structure Verilog-A modules, and generate symbols for your Verilog-A cells for use in a system hierarchy. You also learn to format output data and to use waveform filters to improve simulation performance. In this course, you also examine the AHDL Linter feature to detect potential bugs in the Verilog-A codes.

## Introduction to System and Component Level ESD Protection

**Dr. Joost Willemen** Infineon Technologies AG, Munich

**Filippo Magrini** Infineon Technologies AG, Munich

- Introduction to ESD
- Testing of ESD robustness of systems and components
- Avoiding ESD in production environments
- ESD failure modes
- Design of ESD robust systems
- ESD protection at component level: goals and strategies
- ESD design window definition
- Self-protection vs. non self-protection approach
- Basic ESD device types and physics
- Transistor electrical SOA (Safe Operating Area) and active clamps
- Mixed voltage class ESD protection design

- EDA tools for ESD concept verification and troubleshooting
- Robustness of ESD protection devices with respect to the Wunsch-Bell theory (thermal failure power vs. pulse duration)

## Device Mismatch Characterization: Basics, Test Structures, Measurements, Modelling

**Werner Posch** ams AG

The talk starts with fundamental terms of variability and proceeds with device mismatch characterization in detail. Specific requirements regarding test structures, measurements, statistics and design environment implementation are presented for FETs, BJTs, resistors and capacitors.

## Robust Design of Smart Power ICs for Automotive Applications

**Luca Petruzzi** Infineon Technologies AG, Villach

**Paolo del Croce** Infineon Technologies AG, Villach

Smart power switches are used in various automotive applications to drive different kind of actuators, like e.g. motors, lamps, LED modules. Besides these classical applications, the newest trend for switches in the automotive field is visible in the power distribution system, where they more and more replace the classical fuses and the mechanical relays. Particularly high side switches with very low resistive values (in the range of some tenths of mΩ) find large application in high power automotive systems.

Typical challenges designing such high voltage and high power automotive switches are:

- Developing floating gate driver circuits for power DMOS transistors
- Transferring the information from the low voltage CMOS control circuitry to the floating drivers
- Dealing with high operating currents (10A DC) and very high transient current (up to 100A)
- Designing protections circuits, such as temperature protections, current limitation, overvoltage protections etc., in order to ensure system robustness
- Performing an accurate current sensing, to inform the central microcontroller about the system status (diagnosis functionality)